AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor device, comprising:

a plurality of spaced apart through electrodes with equal cross-sectional areas in a semiconductor chip, which through electrodes electrically link ~~linking~~ a front surface of the chip to a back surface of the chip, wherein

at least two ~~first number~~ of the plurality of through electrodes ~~being electrically~~ are connected to one another to form a first high-current through electrode that ~~which links the front and back surfaces of the chip and~~ is in communication with a power supply,

at least another two ~~second number~~ of the plurality of through ~~hole~~ electrodes are ~~being electrically~~ connected to one another to form a second high-current through electrode that ~~which links the front and back surfaces of the chip and~~ is in communication with ground, ~~and wherein~~

a particular signal-routing through electrode is formed of only one of the plurality of through electrodes; and

at least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated from the chip. ~~wherein at least one of the first number and the second number is two or greater, so that at least one of the first high-current through electrode and the second high-current through electrode is made up of at least two of the through electrodes which are electrically connected to one another~~.

2. (Original) The semiconductor device as set forth in claim 1, wherein at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip.

3. (Canceled)

4. (Currently amended) The semiconductor device as set forth in claim 1, wherein ~~wherein~~ both of the first number and the second number is two or greater, so that each of the first and second high-current through electrodes is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas the signal-routing electrode is made up of only one of the through electrodes.

5. (Previously presented) A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including a semiconductor device according to claim 1.

6. (Canceled)

7. (Previously presented) A chip-stack semiconductor device, comprising:

a plurality of stacked semiconductor chips, each of the semiconductor chips including a number of through electrodes with equal cross-sectional areas therein linking a front surface to a back surface thereof,

wherein at least one of a first high-current through electrode connected to a power supply and a second high-current through electrode connected to ground is made up of at least two of the through electrodes which are electrically connected to one another, whereas a signal-routing electrode connecting a front a back surface of one of the semiconductor chips is made up of only one of the through electrodes, and

at least one of the through electrodes is a non-contact through type electrode which is not electrically connected to the semiconductor chip in which it is formed.

8. (Currently amended) A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including a number of through electrodes with equal cross-sectional areas therein linking a front surface to a back surface thereof, the number of the through electrodes being determined in accordance with a magnitude of an electric current to be conducted therethrough,

wherein

a number of adjacent connected ones of the through electrodes which are connected to a either a ground terminal or a power supply terminal of that semiconductor chip is greater than a number of adjacent connected ones of the through electrodes which are connected to a particular signal terminal thereof, and

at least one of the through electrodes is a non-contact through electrode which is electrically isolated from the semiconductor chip in which it is formed.

9. (Original) The chip-stack semiconductor device as set forth in claim 5, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is

greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

10. (Canceled)

11. (Original) The chip-stack semiconductor device as set forth in claim 7, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

12. (Original) The chip-stack semiconductor device as set forth in claim 8, wherein a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

13. (Previously presented) The chip-stack semiconductor device as set forth in claim 5, wherein the first and second number of the through electrodes is increased as an interconnect line length through the multiple stacked semiconductor chips is increased.

14. (Canceled)

15. (Previously presented) The chip-stack semiconductor device as set forth in claim 7, wherein the first and second number of the through electrodes is increased as an interconnect line length through the multiple stacked semiconductor chips is increased.

16. (Previously presented) The chip-stack semiconductor device as set forth in claim 8, wherein the first and second number of the through electrodes is increased as an interconnect line length through the multiple stacked semiconductor chips is increased.

17. (Previously presented) The chip-stack semiconductor device as set forth in claim 13, wherein the first and second number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

18. (Canceled)

19. (Previously presented) The chip-stack semiconductor device as set forth in claim 15, wherein the first and second number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

20. (Previously presented) The chip-stack semiconductor device as set forth in claim 16, wherein the first and second number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.